We claim:

1. A multiple-clock-domain microprocessor comprising:

a plurality of domains; and

for each of the plurality of domains, a clock for separately generating a clock signal for that domain.

2. The microprocessor of claim 1, wherein each said clock comprises a phase-locked loop, and wherein the microprocessor further comprises means for receiving an externally generated clock signal and for supplying the externally generated clock signal to each said phase-locked loop.

3. A method of operating a microprocessor, the method comprising:

providing a plurality of domains in the microprocessor;

clocking each of the domains separately; and

operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another.